A novel back gate biasing technique for power efficient SOC in FDSOI technology node

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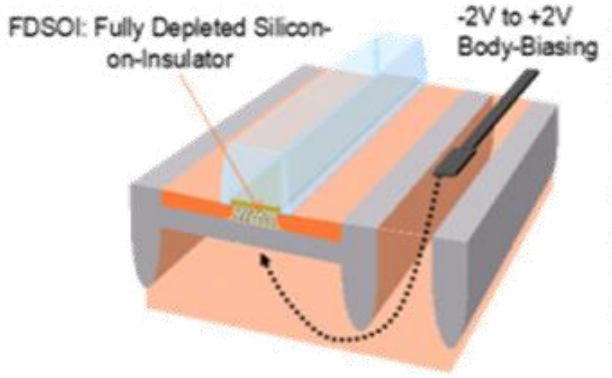
MOTIVATION

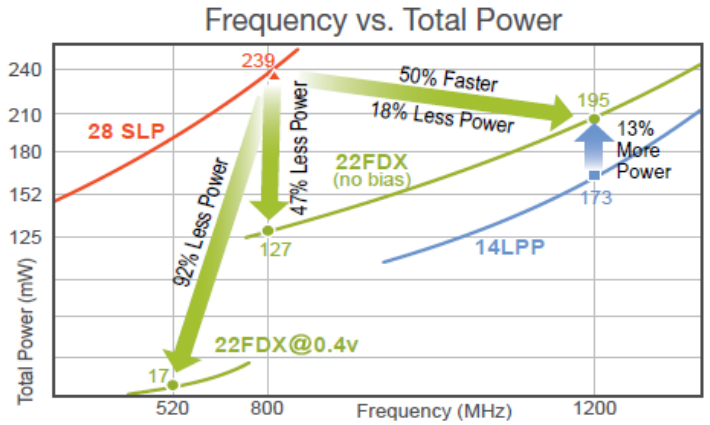
FDSOI technology has enabled the semiconductor industry with an unique feature of **body biasing** and **improving PPA efficiency** compared to conventional bulk technologies.



Architected for Effective Back-gate Biasing

Technology back-gate biasing feature enables dynamic tradeoffs between power, performance and leakage and provides the greatest design flexibility.

High Performance and Low Power



Forward Body Bias (FBB)

- 50% lower power at same frequency (vs 28nm)
- Up to 40% faster performance at same power (vs 28nm)

Reverse Body Bias (RBB)

- Reduces leakage to 1pA/micron in standby mode

Popular Choice for

- Low power embedded applications
  - + 5G: <6GHz and mmWave handset solutions, backhaul, base stations
  - + LEO satellite communications
  - + mmWave radar
  - + Narrow-band IoT, Wearables
  - + Mobile Applications Processors
  - + Networking and WiFi
  - + Automotive (ADAS, IVI)

IMAGE COURTESY: https://www.globalfoundries.com/sites/default/files/product-briefs/22fdx-product-brief_0.pdf

Back gate control mechanism in 22FDX technology has matured enough and now commercially available.
The **concept is proven** and **production ready**.

Designers have started leveraging these differentiated features and demonstrated **novel architectural** solutions for **better FoM**.

With forward back gate biasing and reverse back gate biasing, circuit designers can align the critical design specs with **minimal power** and **area overhead,** however this **needs architectural adjustment**.

OBJECTIVE : Provide an **architectural solution** for **power efficient SoC** with **dynamic power** and **performance scaling** utilizing **body biasing** for both analog and digital core components.

PROBLEM STATEMENT

- **Need Design Methodology** for most **power efficient solution** within SOC **utilizing BODY BIASING**.
- **Need** Adaptive **BODY BIASING** for **analog** and **digital** core components for **dynamic power** and **performance scaling**.
- During production testing in ATE, analog sub-systems need calibration and alignment for best yield across wider number of samples.

  Need to **reduce** the **extra cost** and **time to market** involved with conventional method of alignment using external components and some cases considerable tester time.

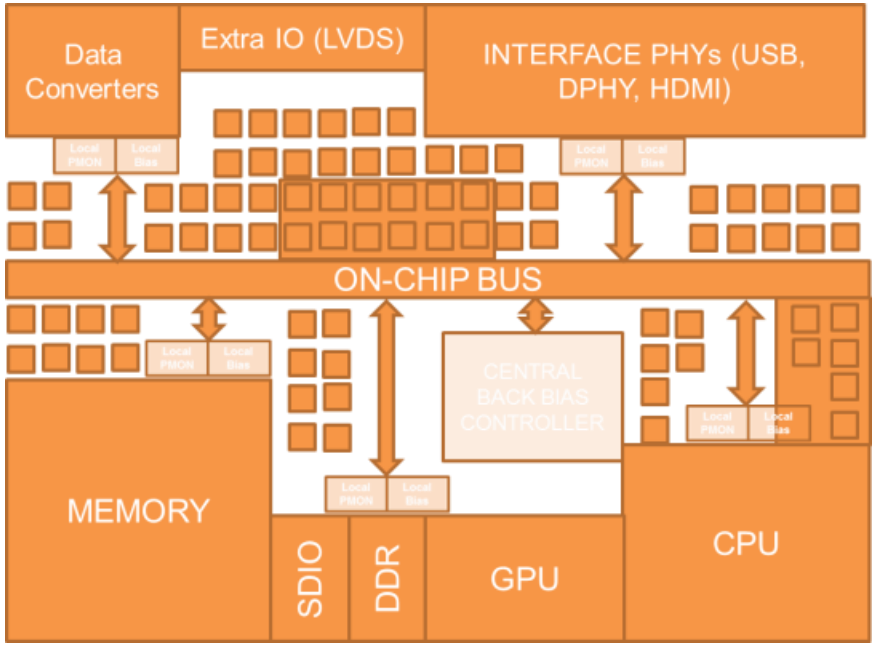
PROPOSED SOLUTION

Deliver an architectural solution with back gate bias control that helps the IC / SOC production house with

- ❑ **Lower testing/ bring up cost**
- ❑ **Faster time to market**

BY PROVIDING : Trimming which would be adaptive in nature by dynamically adjusting the back gate bias node and align performance at the desired range for highest yield and reliability.

BY UTILISING : A novel body biasing scheme with local bias nodes and PVT monitoring points for analog / digital components in a SOC with negligible power and area penalty.



Proposed Solution

TARGET DESIGNS

ADDITIONAL BLOCKS of PROPOSED SOLUTION. Explained on NEXT Slide

PROPOSED SOLUTION

A novel scheme within a SOC for dynamic biasing and PPA optimization

COMPONENT DESCRIPTION

Back bias controller (BBC)

- Can be placed at a convenient location of the SOC.
- Decodes process info and other user defined input parameters.
- Provides back gate bias code for the macros in SOC that use back gate bias operation for PPA improvements.
- Designed with PVT correlation algorithm. The algorithm is macro specific and different best fit curves would be drawn for specific designs.

Local PVT monitors (LPMON)

- Provide process, voltage and temperature info closer to analog / digital macros to the central controller (BBC).
- Apart from global process info, local process monitor also captures local mismatch trend.
- Type of PMON are specific to the Macro and designed based on functionality of the block (CMOS, Resistor, capacitor, IO devices etc).
- Junction temperature sensor captures local temperature within +/-5^{0}C range.
- Local core voltage monitors are used to take out dependencies from IR drop.

Local bias generator (LB)

- Used to generate positive and negative voltages for forward and reverse body bias operation. This block functions as a DAC.
- Input of the DACs come from BBC and LB drives local N/P wells accordingly.

Signal FLOW DIAGRAM

BBC enables the Local PMON using ENABLE signal

↓

LPMON provides the PVT info closer to analog / digital macros to BBC on the PMON DATA bus

↓

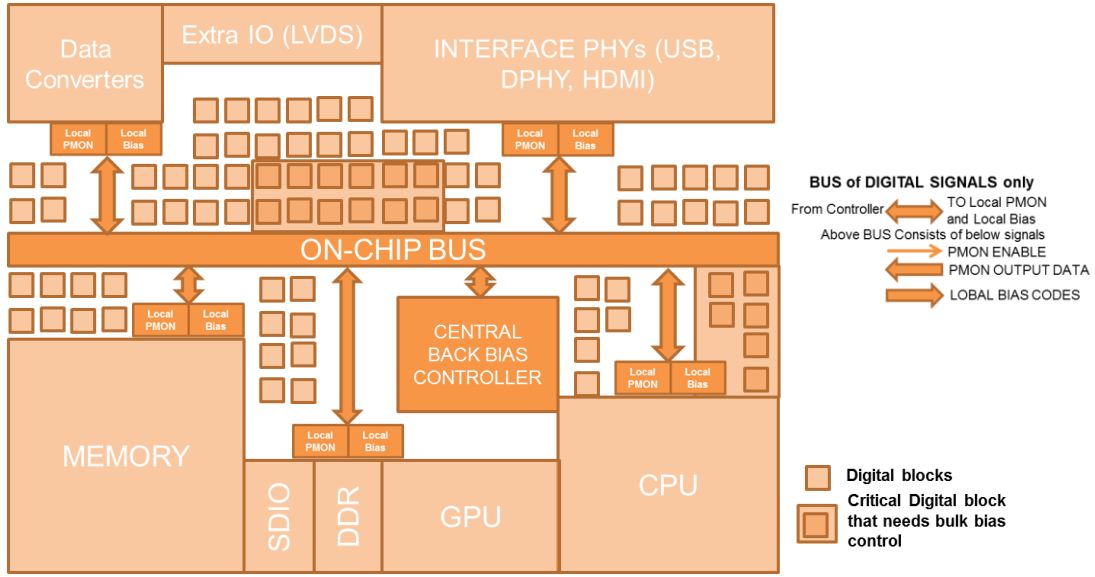
BBC sends Bias Codes to Local Bias Generators based on correlation algorithm which is macro specific

↓

LB generates +ve and –ve voltages to bias the macro well areas

↓

Body bias control mapping data from controller for each local bias nodes may be programmed in ROM/ OTP or Fuse during production testing



ALL communication between BBC and LB + LPMON are digital in nature and can be programmed to take place only during production boot phase at a lower speed. The digital only routing is SOC friendly.

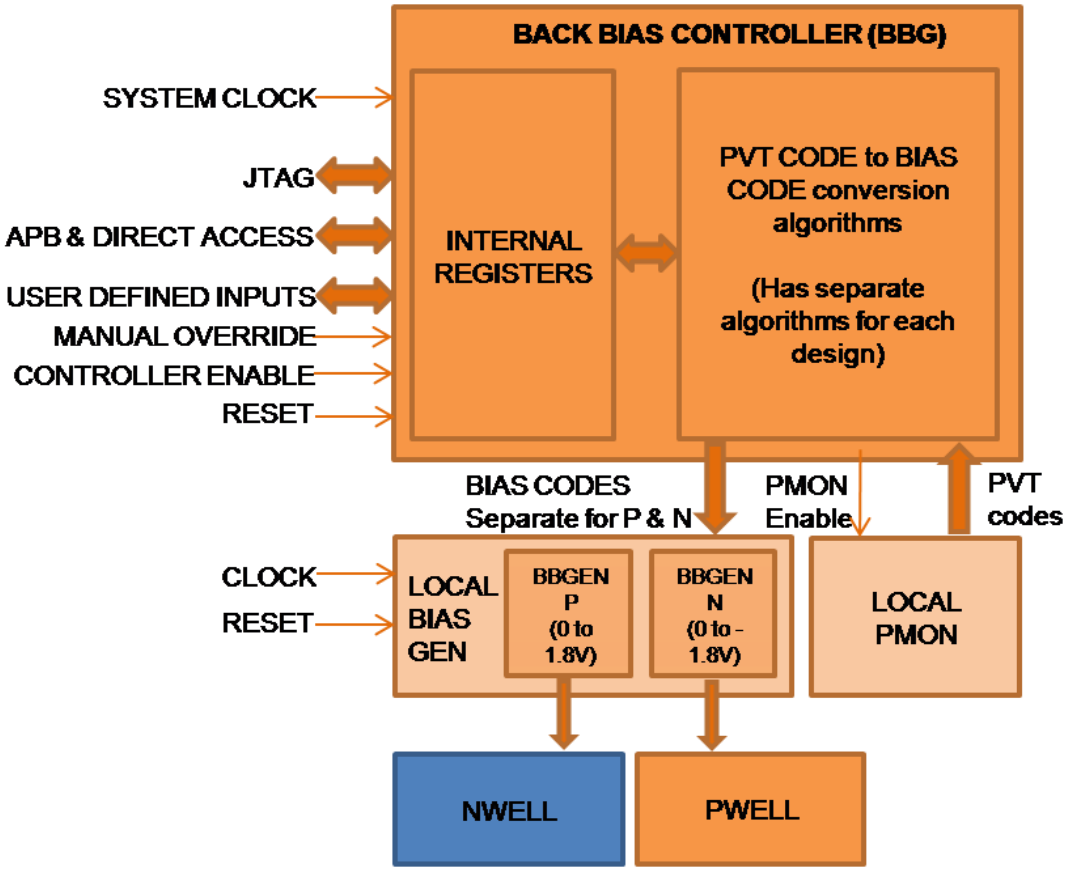
ADDITIONAL BENEFITS

Apart from trimming of process spread for critical sensitive analog / digital components, one can control PPA of an analog system as well by body bias control. (For this user needs to enable low power mode operation)

Overall area and power impact of the additional controller and local bias nodes would be negligible compared to the utility and value addition

BACK BIAS CONTROLLER (BBC)

BACK BIAS CONTROLLER BLOCK DIAGRAM



PVT Codes Consist of

1. P_CODE from Custom PMON
2. T_CODE from Temp Sensor
3. V_CODE from Voltage Sensor

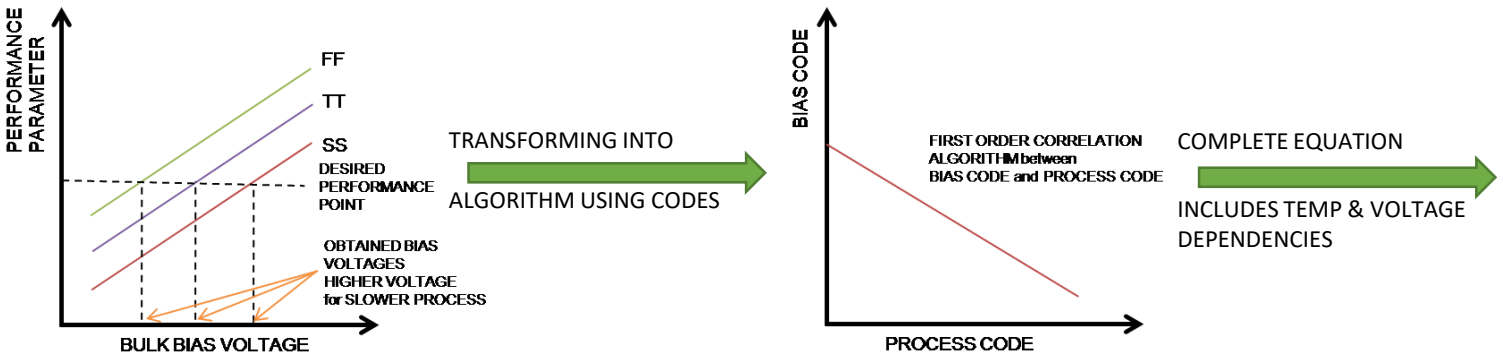
COMPONENT DESCRIPTION

Back bias controller (BBC)

- Can be placed at a convenient location of the SOC.
- Decodes process info and other user defined input parameters
- Provides back gate bias code for the macros in SOC that use back gate bias operation for PPA improvements.
- Designed with PVT correlation algorithm The algorithm is macro specific and different best fit curves would be drawn for specific designs.
- Algorithms can be hard coded or software controlled.
- Provides option of one time calibration during bring up phase for less sensitive analog or digital components.
- Provides option of periodic calibration for highly sensitive components.

BACK BIAS CONTROLLER (BBC)

ILLUSTRATING HOW BIAS CODE IS OBTAINED FROM PROCESS CODE



EQUATION (1)

$$BIAS\_CODE = (SLOPE\_P * P\_CODE + OFFSET\_P) + (SLOPE\_T * T\_CODE + OFFSET\_T) + (SLOPE\_V * V\_CODE + OFFSET\_V)$$

SLOPE and OFFSET for Temp & Voltage terms can be Dependent on P_CODE

Performance Plot of a circuit (Ex. Frequency of a RING OSCILLATOR) vs BULK VOLTAGE is shown above.

For different process, different BULK VOLTAGE is needed to either BOOST or REDUCE the performance to align towards TYPICAL performance

BIAS CODE vs PROCESS CODE is shown above.

Lower PROCESS CODE means SLOWER process and higher CODE means FASTER process.

BIAS CODE is sent to LOCAL BIAS GENERATOR (LB) to generate the BULK VOLTAGE which needs to be applied to the circuit.

SLOPE and OFFSET terms are derived from simulations for each circuit.

The ALGORITHM can be a **LINEAR MODEL** or a **PIECE-WISE LINEAR MODEL** for **second order relationship** curves between performance parameter and bulk voltage

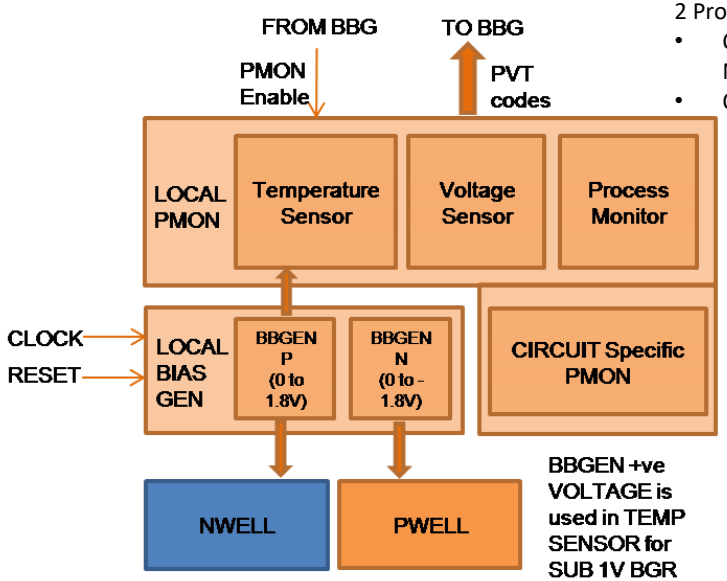
LOCAL PMON (LPMON)

COMPONENT DESCRIPTION

Local PVT monitors (LPMON)

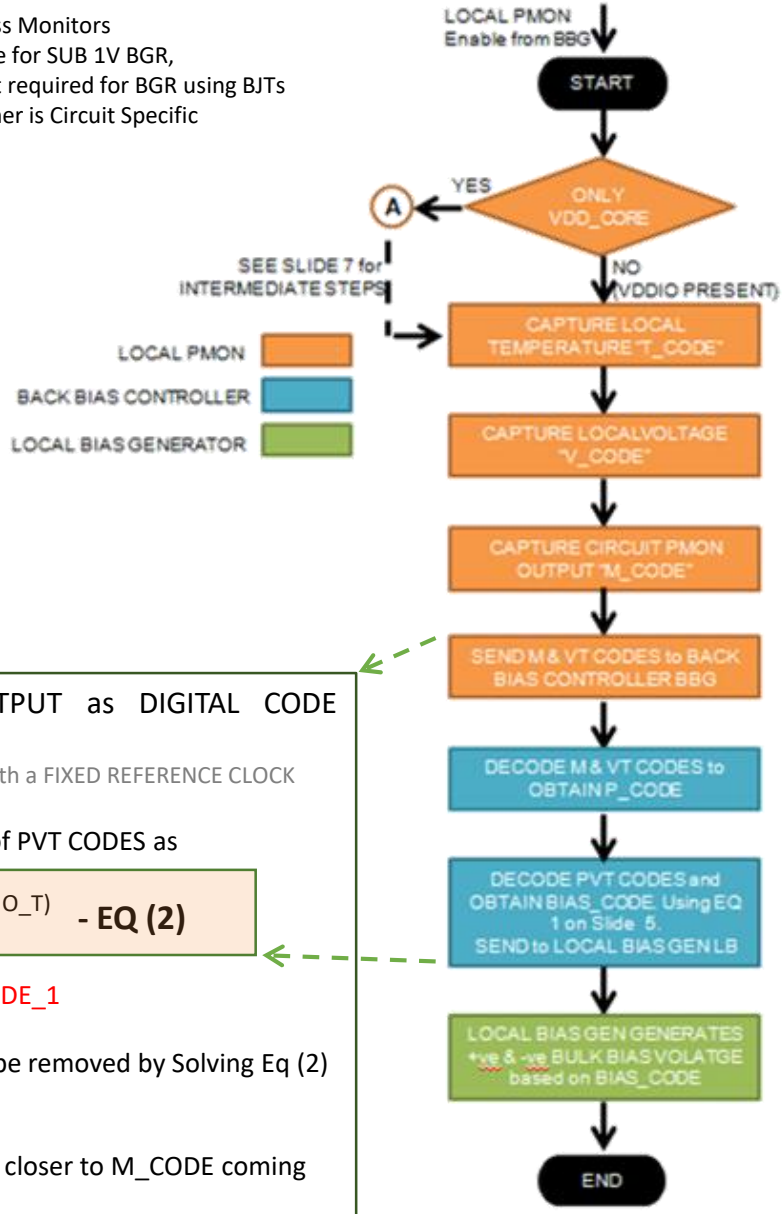
- Provide process, voltage and temperature info closer to analog/ digital macros to the central controller (BBC).
- Apart from global process info local process monitor also captures local mismatch trend.
- Type of PMON are specific to the Macro and designed based on functionality of the block (CMOS, Resistor, capacitor, IO devices etc).
- Junction temperature sensor captures local temperature within +/- 5^0C range.
- Local core voltage monitors are used to take out dependencies from IR drop.

LOCAL PMON BLOCK DIAGRAM



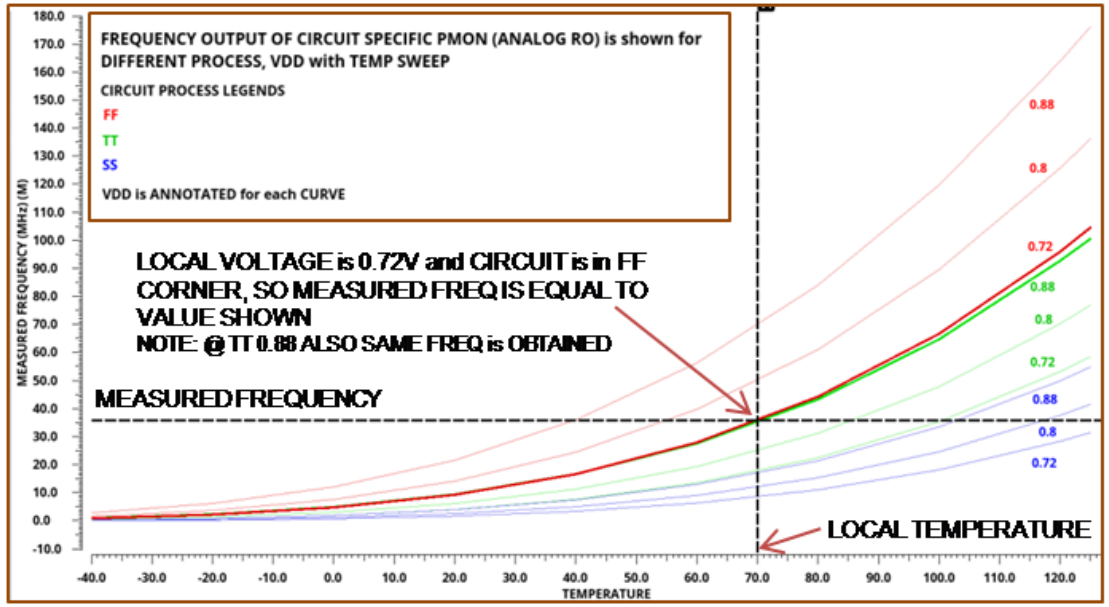
2 Process Monitors

- One for SUB 1V BGR,
  Not required for BGR using BJTs
- Other is Circuit Specific



LPMON FLOW DIAGRAM

ILLUSTRATING HOW PROCESS CODE IS OBTAINED FROM CIRCUIT SPECIFIC PMON OUTPUT



➢ CIRCUIT SPECIFIC PMON provides OUTPUT as DIGITAL CODE (M_CODE)

Ex. FREQ is converted to DIGITAL CODE using COUNTER with a FIXED REFERENCE CLOCK

➢ Obtained M_CODE can be EXPRESSED in terms of PVT CODES as

$$M\_CODE = (S\_P * P\_CODE + O\_P) + (S\_T * T\_CODE + O\_T) + (S\_V * V\_CODE + O\_V) \quad \text{- EQ (2)}$$

➢ SOLVE FOR P_CODE, This is 1st Order value P_CODE_1

➢ 2nd Order dependencies of Temp & Voltage can be removed by Solving Eq (2) for M_CODE_expected using P_CODE_1.

➢ Choose P_CODE for which M_CODE_expected is closer to M_CODE coming from PMON

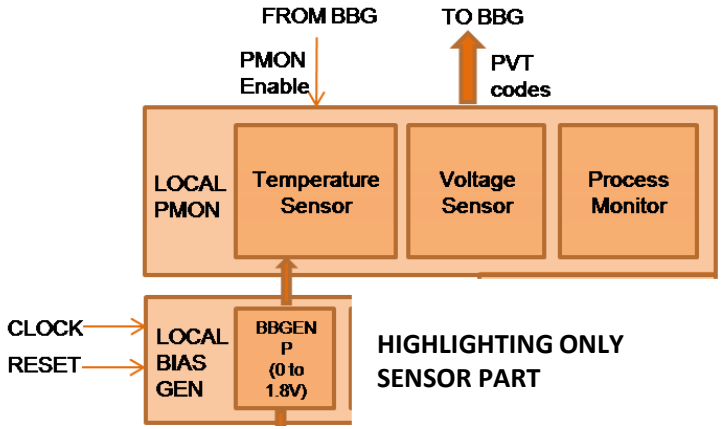
LOCAL PMON (LPMON) – PVT SENSOR

COMPONENT DESCRIPTION

TEMPERATURE SENSOR

- Uses only VDD_CORE Supply
- **Junction temperature sensor captures local temperature within +/- 5^{0}C range.**
- Uses +ve BULK voltage for calibrating MOS diodes to capture temperature
- Custom PMON structures capture process code of MOS diode and resistor used within core of the TS/ VS
- PMON output freq. vs process code is a pre-defined equation which would be written with controller program
- Local BBGEN to be used during TS / VS calibration, once the temp and voltage codes are captured in central back bias controller

LOCAL PMON BLOCK DIAGRAM

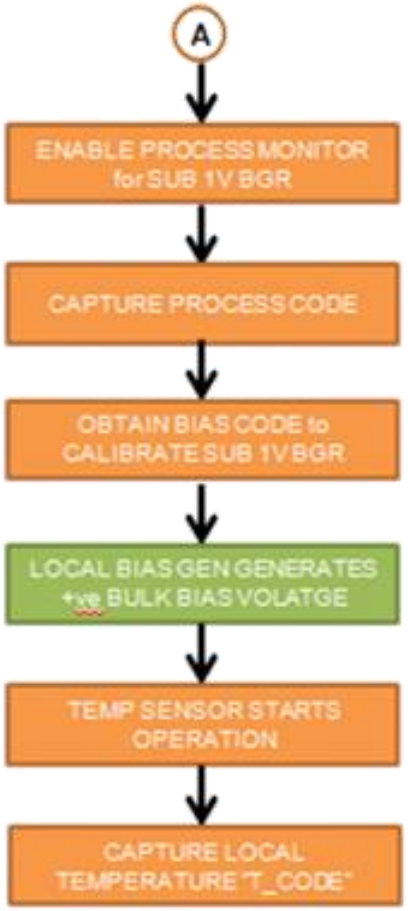


HIGHLIGHTING ONLY SENSOR PART

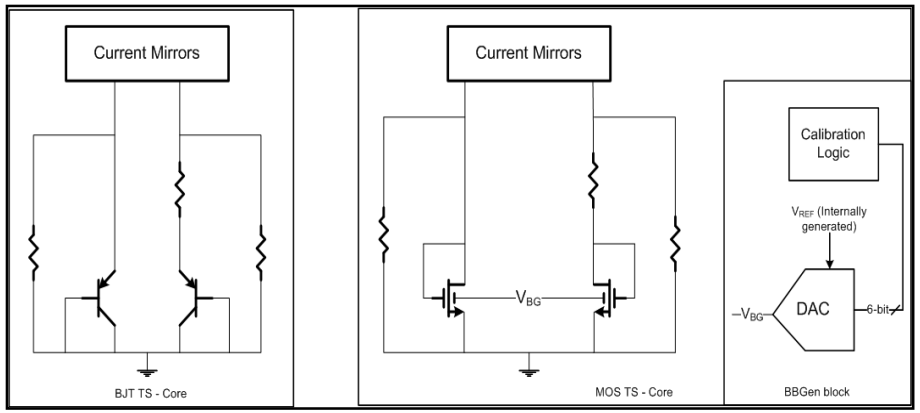
2 Process Monitors

- One for SUB 1V BGR, Not required for BGR using BJTs
- Other is macro critical component specific

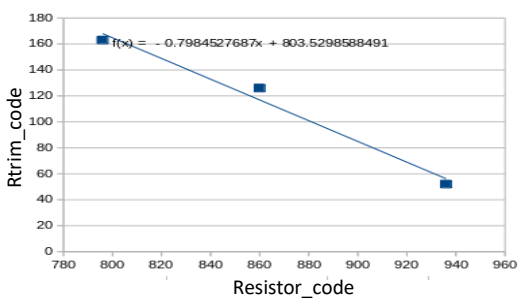
TEMP SENSOR FLOW DIAGRAM

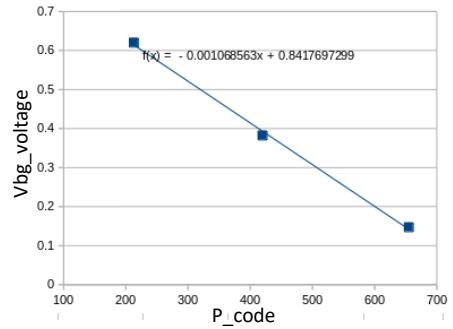


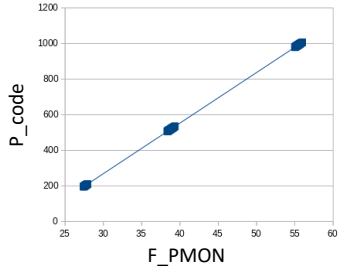
REFERENCE GENERATION CIRCUIT in TEMPERATURE SENSOR



- SUB 1V BGR requires calibration to obtain +ve BULK VOLTAGE for correct operation.
- If VDDIO domain is available, regular BGR using BJTs can be used which does not requires calibration



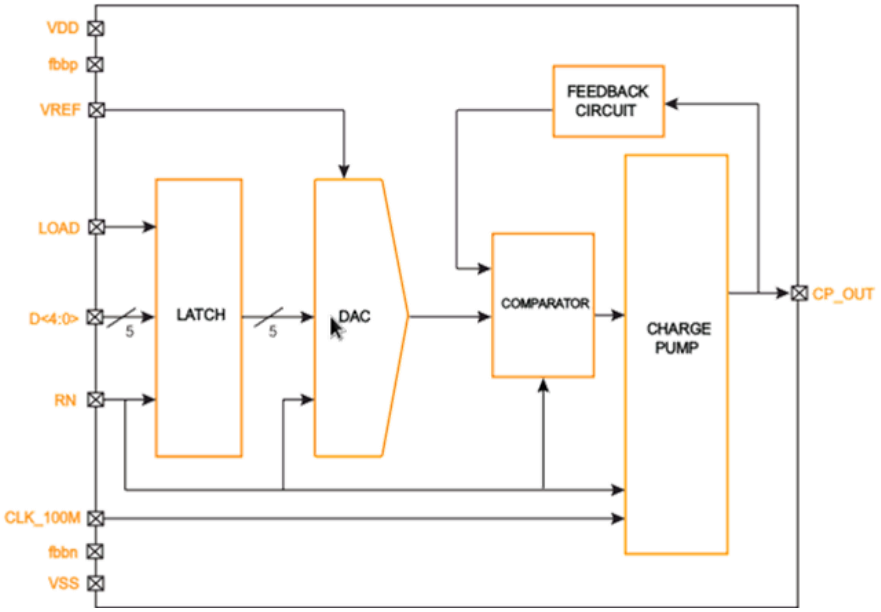




T_sensor	W/O BB	With BB MOS
Area	0.025	0.024
Power	0.5mW	0.25mW
Accuracy	+/- 7C	+/- 5C

LOCAL BIAS GENERATOR (LB)

LB BLOCK DIAGRAM



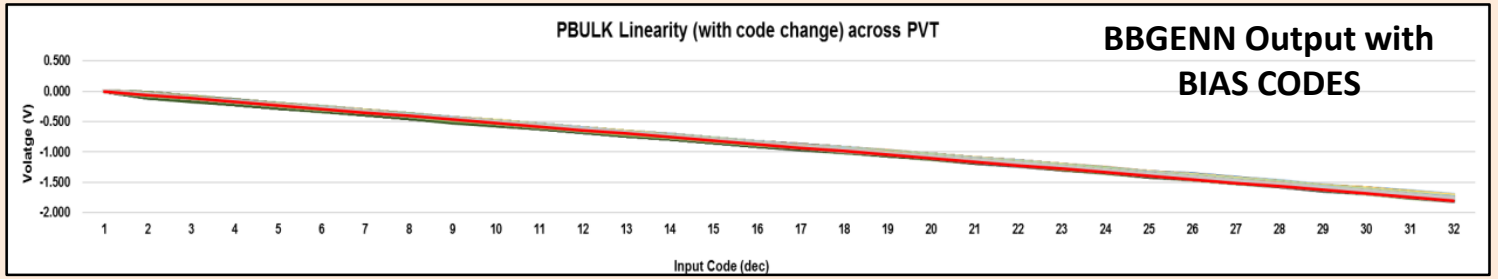
The LOCAL BODY BIAS GENERATOR consists of :

- LATCH and DAC to store BIAS codes and generate a reference voltage for next stage
- COMPARATOR and CHARGE PUMP to form a closed loop to support varying load conditions

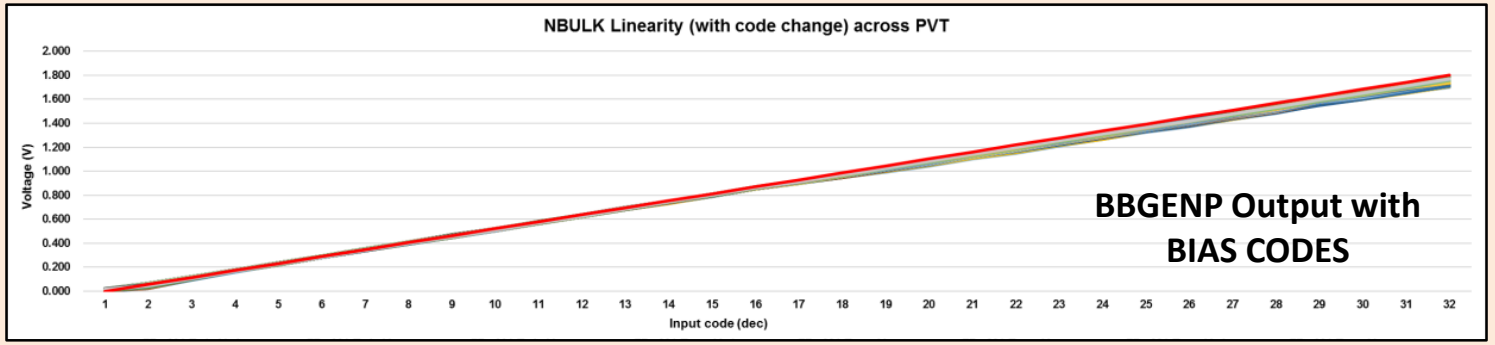
The BBGEN produces output voltage in range on 0 to +/- 1.8V to utilize the full range of body biasing through 22FDX technology.

Reference voltage used would be same as core voltage of 0.8V

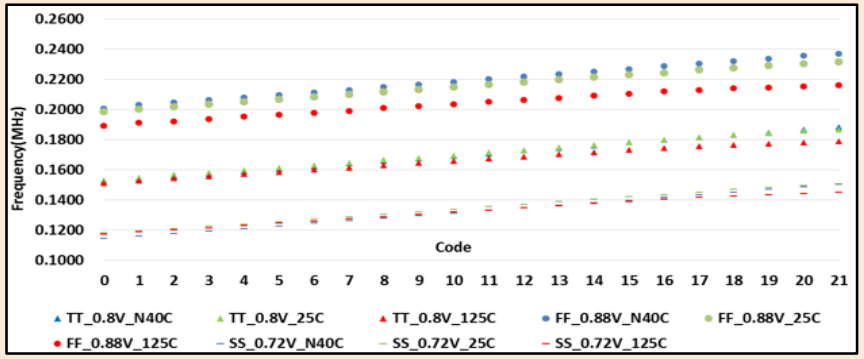
Local Bias generator Silicon Results



BBGENN Output with BIAS CODES



BBGENP Output with BIAS CODES

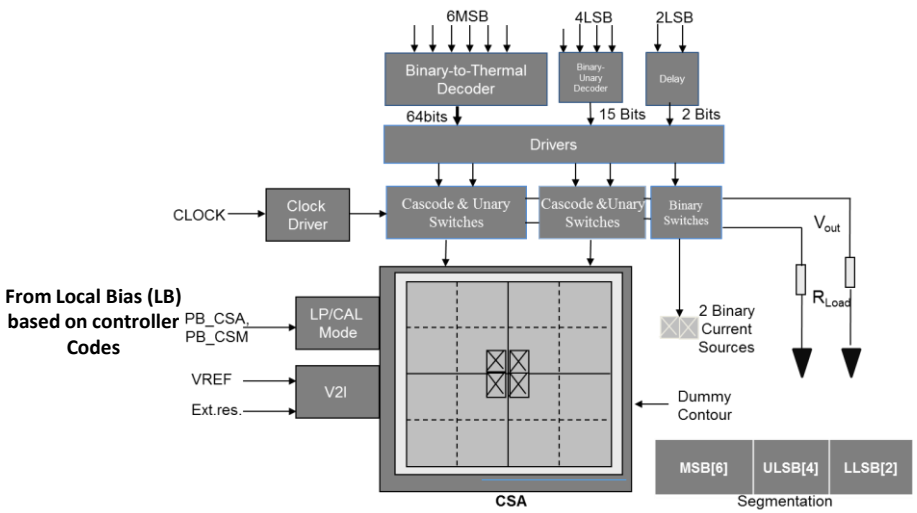


EFFECT of BULK VOLTAGE

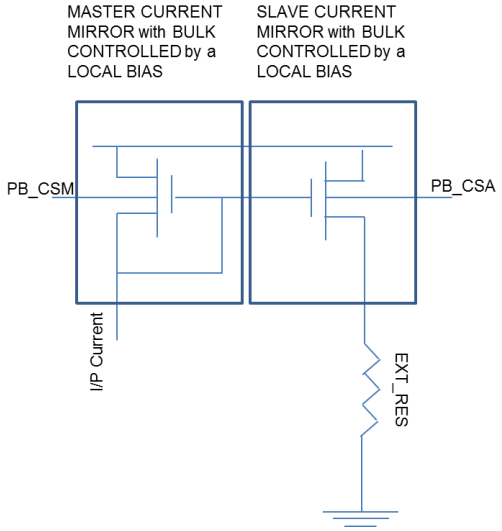
RO Frequency vs BIAS Code
RO from Core using LVT C28 library

DESIGN BIASED	WELL AREA BIASED	AREA OVERHEAD	POWER OVERHEAD / POWER
STD CELL LOGIC	10mm^2	0.5%	-
5 LANE MIPI DPHY	0.4mm^2	0.2%	< 0.1%

Use case: 12b 300Msps DAC with body bias

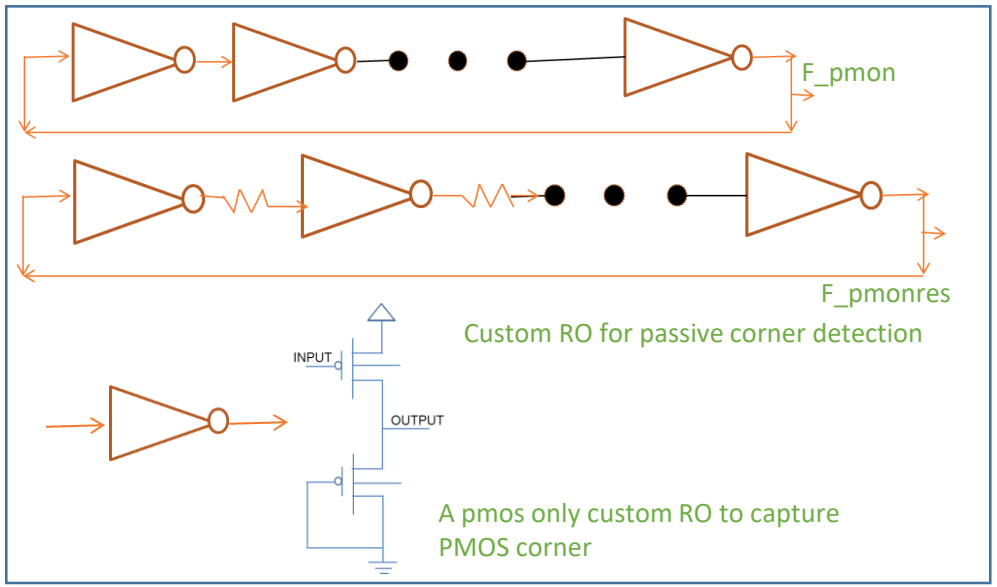


Video DAC block diagram



Unit current cells of DAC with back gate control

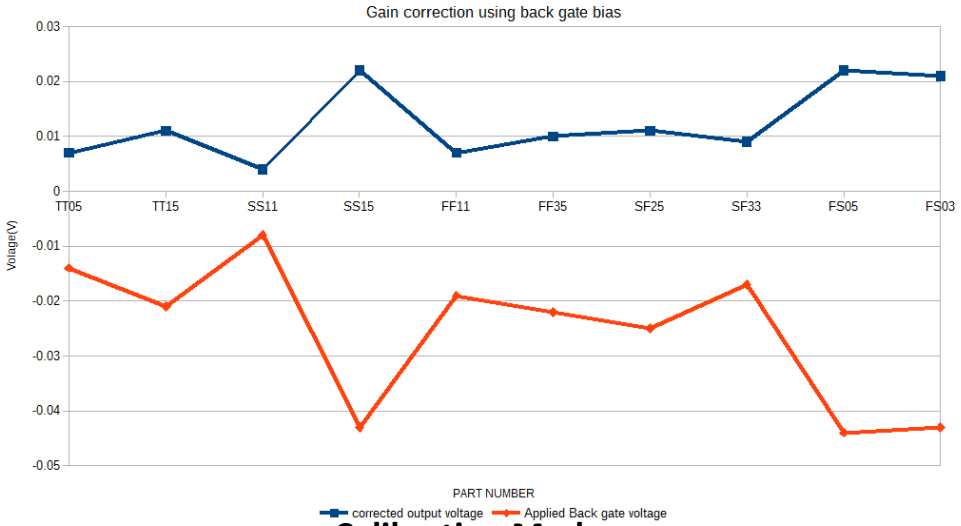
For the DAC under test, unit current defining cell (master) and mirrored slave branches are present in separate well areas and based on power and performance requirement these will be controlled together or independently as follows.



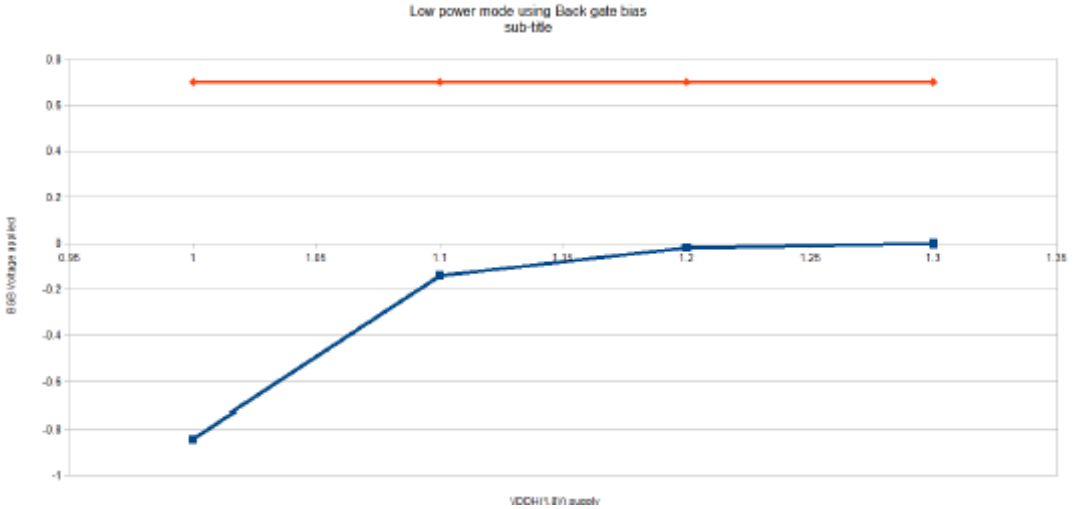
Low Power Mode	Calibration ON
LB1==LB2, Change the bulk bias based on process information to get typical performance and power	PMON analog input to be used for controlling any of LB1 or LB2 or both to improve linearity and noise by reducing the mismatch arisisng between the master and slave currents

12b 300Msps DAC SILICON RESULTS

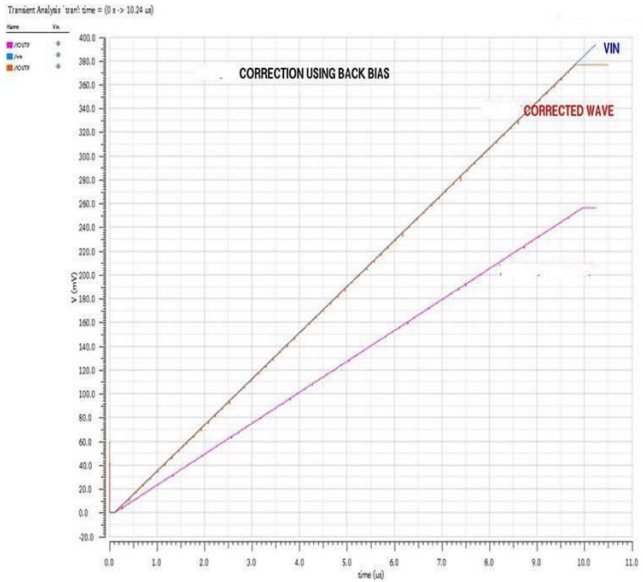
BULK BIAS VOLTAGE FOR DAC ON SILICON FOR DIFFERENT PARTS



Calibration Mode



Low Power Mode



Corrected gain error of VDAC using FBB

Limitation – HF ripple with bias node

- Ripple with bias mesh would be critical for precision application.
- User need to take an account for the noise and accordingly impact with performance specification
- Low pass filtering would be a convenient solution before using the bias

E.G: DAC output load 10pF, 10K Full scale reference is measured for 12b DAC Attenuation wrt full scale signal of 1V

Noise 10mV @	Output ripple	Attenuation
5KHz	6.5mV	-43dB
10MHz	8.6mV	-41dB
100MHz	7.5mV	-42dB

CONCLUSION

- A novel adaptive back gate biasing scheme demonstrated for efficient usage of FBB (Forward back gate biasing) and RBB (Reverse back gate biasing) for best power efficient SOC design
- Using a central controller and local bias nodes analog/ digital subsystems are self aligned with best FoM improvement and yield.
- The body biasing design methodology involves all digital signal routing across the SOC and enabling calibration automation during production testing
- A high speed DAC designed and implemented with back gate bias usage. The low power mode can operate at 40% lesser supply while achieving similar performance and in calibration mode the design can align itself within best yield margin
- Critical path ROs have been taken as performance monitor to align a processor to its best power and performance matrix using the back gate biasing scheme
- While the body bias generator controller scheme provides excellent return on investment, the fundamental body bias control of the body node is now production proven
- The concept of adaptive biasing is silicon proven and used to reduce production cost and faster time to market
- Future Scope of work: Implementation of the whole approach in production (Work in progress)